REMARKS

This amendment responds to the office action mailed June 17, 2003. In the office action the Examiner:

- allowed claims 1-15, 21 and 22;
- objected to claims 19 and 20 for containing informalities; and
- rejected claim 16 under 35 U.S.C. 102(e) as being anticipated by Hassoun et al., U.S. Patent No. 6,289,068;
- rejected claims 19 and 20 under 35 U.S.C. 103(a) as unpatentable over Hassoun et al., U.S. Patent No. 6,289,068 in view of applicant's admitted prior art Figure 5; and
- rejected claims 17 and 18 as being dependent upon a rejected base claim.

After entry of this amendment, the pending claims are: claims 1-22.

REMARKS CONCERNING REVISED FIGURES

Figures 1A, 1B, 2, 3, 4, and 5 have been revised by adding the legend "PRIOR ART", as requested by the Examiner. Replacement Sheets for these Figures are attached hereto, in Appendix A.

The Examiner is respectfully requested to approve the proposed drawing changes.

Figure 6 has not be revised, because Figure 6 shows ideal phase relationships not achieved by any prior art known to applicant.

REMARKS CONCERNING CLAIMS

Claim 16 was amended (in its preamble) to clarify that the second system clock is a signal communicated by the channel away from the master.

Claim 20 was amended to correct an antecedent reference error.

Claims 1, 10, 12 and 21 were revised by adding the word "and" before the last element.

Many of the claims have been revised for clarity.

Claims 19 and 20

Contrary to the Examiner's objection, claims 19 and 20 are supported by the specification. With regard to claim 19, the tclk signal is used in Figures 7 and 8 to clock the Output Drivers 24. Please note that in Figures 7 and 8, element 22a is a buffer, not an inverter; see the specification on page 8, line 16. Thus, it is the transmit clock, and not its complement, that is used to enable (or clock) the output drivers in the embodiments shown in Figures 7 and 8.

With regard to claim 20, the use of the "complement of a receive clock" to enable the output drivers is supported by the specification, starting at page 9, line 1, where it is stated:

> The exemplary circuits shown above may be modified to operate by **using the complement of rclk, rather than tclk to control the output drivers.** Since the feedback loop in the circuits above aligns tclk to the complement rclk, either signal may be used to control the transmit circuitry. Where the complement of rclk is used as the controlling signal, tclk exists merely to produce CFM.
> (emphasis added)

For these reasons, the applicant requests that the objections to claims 19 and 20 be withdrawn.

Claim 16 vs. Hassoun et al. (6,289,068)

Unlike claim 16, Hassoun does not provide "a 90° block configured to receive the transmit system clock and to generate a 90° phased shifted version of the transmit clock signal". There are at least two reasons why this is so.

First, the only 90° blocks provided by Hassoun are within the clock phase shifter 350 of the DLL 300, whereas claim 16 requires a 90° block that receives a "transmit clock signal" generated by the DLL. As can be seen in Figures 3, 6 and 7 of Hassoun, the output signal generated by the Hassoun DLL 300, called the O_CLK, is never received by a 90° block - represented by the delay lines 610 and 710 in Hassoun's Figures 6 and 7. From another viewpoint, the only signals that are inputs to the 90° blocks in Hassoun are signals that are never used as a transmit clock signal.

Second, the term "transmit clock signal" must be construed consistently among all the pending claims. In claim 19, for instance, the transmit clock signal is used to enable a plurality of data output drivers. Thus, the transmit clock signal must be a signal suitable for enabling or clocking the transmission of data. None of the signals received by 90° blocks in Hassoun are disclosed in Hassoun as being suitable or usable as a transmit clock signal.

Thus, Hassoun does not teach or suggest a "90° block" as required by claim 16, and therefore Hassoun does not anticipate claim 16.

Claim 16 also requires an output driver that receives a "90° phased shifted version of the transmit clock signal" and that is configured to generate a "second system clock." The only circuit in Hassoun that could possibly be an output driver is the "logic circuits 190". The "clock skew 180" is not a circuit, as it simply represents the affect of signal propagation on a clock signal. The only other circuit shown in Hassoun is the DLL 300, which is not a candidate for the "output driver" element of claim 16.

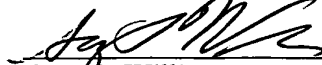
Hassoun does not describe any output signals generated by the "logic circuits 190". In particular, Hassoun does not teach or suggest that the "logic circuits 190" should be used to generate a "second system clock" from a phase shifted version of a transmit clock Furthermore, claim 16 defines the "second system clock" as a clock signal that is generated by an output driver using a phase shifted version of a transmit clock signal. As noted above, the term "transmit clock signal" must be construed consistently across all the pending claims. Thus, the "second system clock" cannot be construed as being any arbitrary clock signal anywhere within a system. Since the output driver circuit is an element of claim 16, Hassoun does not anticipate claim 16.

Claim 19 and 20, which depend from claim 16, are patentable over Hassoun in combination with the admitted prior art of Figure 5 for the same reasons that claim 16 is not anticipated by Hassoun.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at 650 493-4935, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: September 17, 2003



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Appendix A

Revised Figures (see attached copies)